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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/600,050 | 06/20/2003 | Marian Mankos | 10011.001710 (P1100) | 5853 |

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OKAMOTO & BENEDICTO, LLP
P.O. BOX 641330
SAN JOSE, CA 95164

| EXAMINER | |
|---|---|
| HASHMI, ZIA R | |
| **ART UNIT** | **PAPER NUMBER** |
| 2881 | |

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/600,050 | MANKOS ET AL. | |
| | Examiner | Art Unit | |
| | Zia R. Hashmi | 2881 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/10/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under U.S.C. 103(a) as being unpatentable over Lo et al. ( 6,566,897 ), in view of Suzuki et al. ( Pub. No: US 2003/0155508 A1 ).

3. With respect to independent claims 1, 9, 18 and dependent claim 14, Lo et al. disclose a method and apparatus for inspecting a substrate ( Abstract, lines 1-2 and col. 5, lines 17-20 ) comprising: supporting the substrate into a holding place of a substrate holder; moving the substrate holder under the electron beam ( col. 7, lines 40-51 and 14 in Fig. 1 ), applying voltage to the substrate holder ( col. 7, lines 14-30 and 28 in Fig. 1 ), under an electron beam ( 18 and 22 in Fig. 1 ), wherein the voltage applied reduces a substrate edge effect or artifacts ( col. 2, lines 35-67, col. 3, lines 1-3 & 55-59, col. 4, lines 1-8, col. 5, lines 10-12 & 17-20, and 22, 24, 30 & 32 in Fig. 1 ). Their system provides a mechanism for moving a semiconductor wafer holder under an electron beam ( col. 7, lines 40-41, col. 8, lines 5-6, and 14 in Fig. 1 ).

4. With respect to claims 1-13 and 15-20, Lo et al. fail to disclose an isolated conductive element of the substrate holder comprising of an insulating element. Suzuki et al., however, disclose method of applying voltage ( para 0028, lines 9-12 ) to a

conductive element ( para 0030, lines 1-11 ) of the substrate holder ( para 0032, lines 22-24 ), under an electron beam ( para 0024, lines 2-4 ), by means of power supply ( 23 in Fig. 1 ).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to combine methods and apparatus of Lo and Suzuki et al. and add features like adjusting the voltage applied to the conductive element of the substrate holder according the gap size between an edge of the substrate and the holding place in order to reduce the edge effect distortion, which is well known to be eliminated by flooding a larger area by electrons on the sample than is imaged, or by pre-charging an area before moving to another area as practiced by Lo et al. ( col. 5, lines 10-16 ), because Lo et al. teach ( col. 1, lines 56-58 ) that charged particle beam inspection will likely become one of the most critical technologies in advanced semiconductor manufacture.

***Conclusion***

5. Jau et al. disclose ( 6, 710,342 ) a method and apparatus for scanning semiconductor wafers for reducing the edge and aliasing effects in wafer inspections.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zia Hashmi whose telephone number is (571) 272-2473. The examiner can normally be reached between 8.30 AM- 5 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John R. Lee can be reached on (571) 272-2477.

Zia Hashmi

April 3, 2004.

JOHN R. LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800